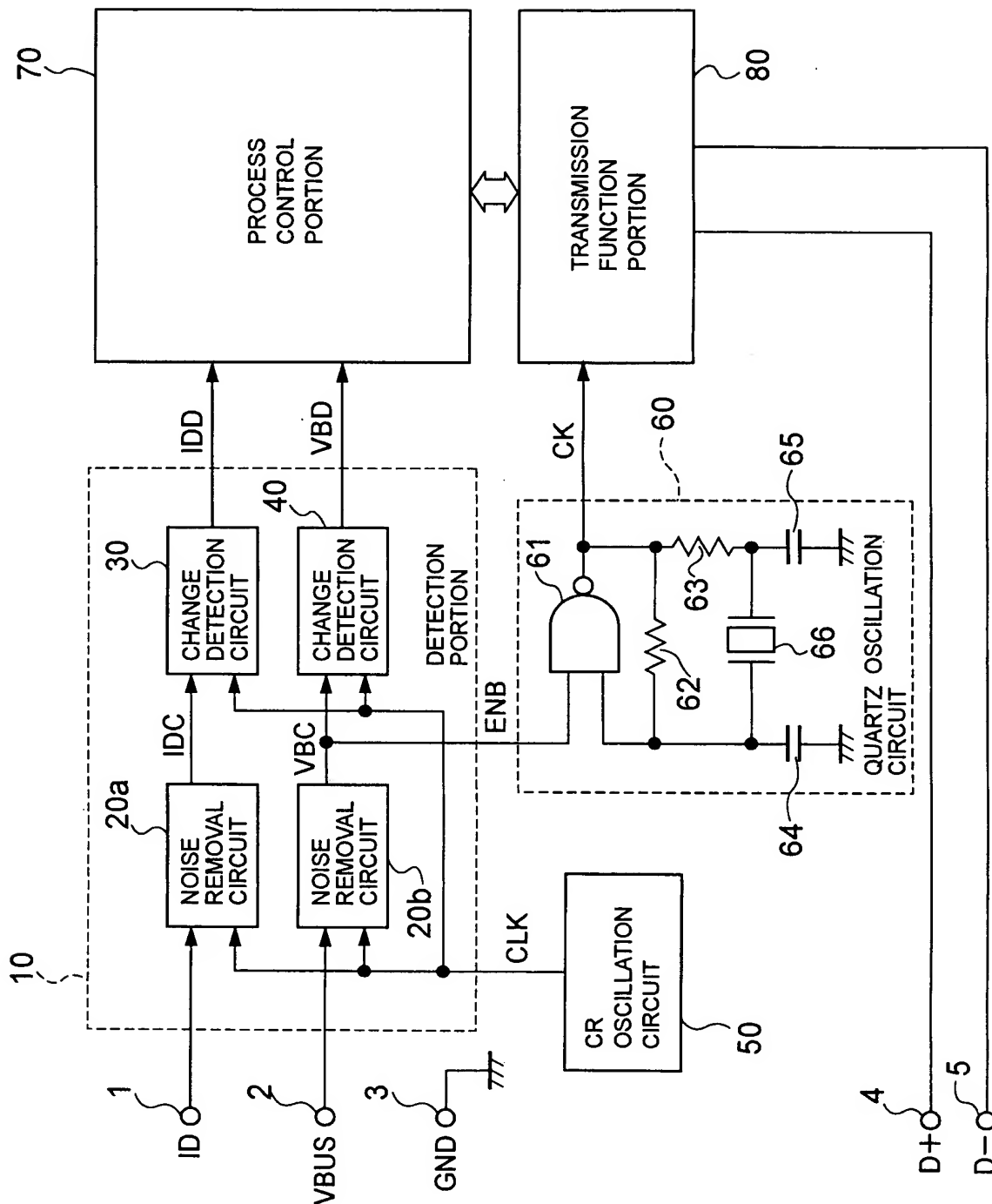




FIG. 1



The diagram shows a digital logic circuit labeled "NOISE REMOVAL CIRCUIT 20". It features three D-type flip-flops (21, 22, 23) and one J-K flip-flop (26). The inputs are ID, VBUS, and CLK. The outputs are IDC and VBC. The circuit is designed to remove noise from the input signals.

The circuit components and their connections are as follows:

- Flip-flops 21, 22, and 23:** These are D-type flip-flops. Their D inputs are connected to ID, VBUS, and CLK respectively. Their Q outputs are connected to the inputs of flip-flop 26.
- Flip-flop 26:** This is a J-K flip-flop. Its J input is connected to the Q output of flip-flop 21. Its K input is connected to the Q output of flip-flop 22. Its clock input (C) is connected to the Q output of flip-flop 23. Its Q output is connected to the output IDC.
- Logic gates:** There are two logic gates, 24 and 25. Gate 24 is an AND gate with inputs from ID and VBUS. Gate 25 is an OR gate with inputs from ID and VBUS. The output of gate 25 is connected to the clock input (C) of flip-flop 26.

CHANGE DETECTION CIRCUIT 30

CHANGE DETECTION CIRCUIT 40

CR OSCILLATION CIRCUIT 50

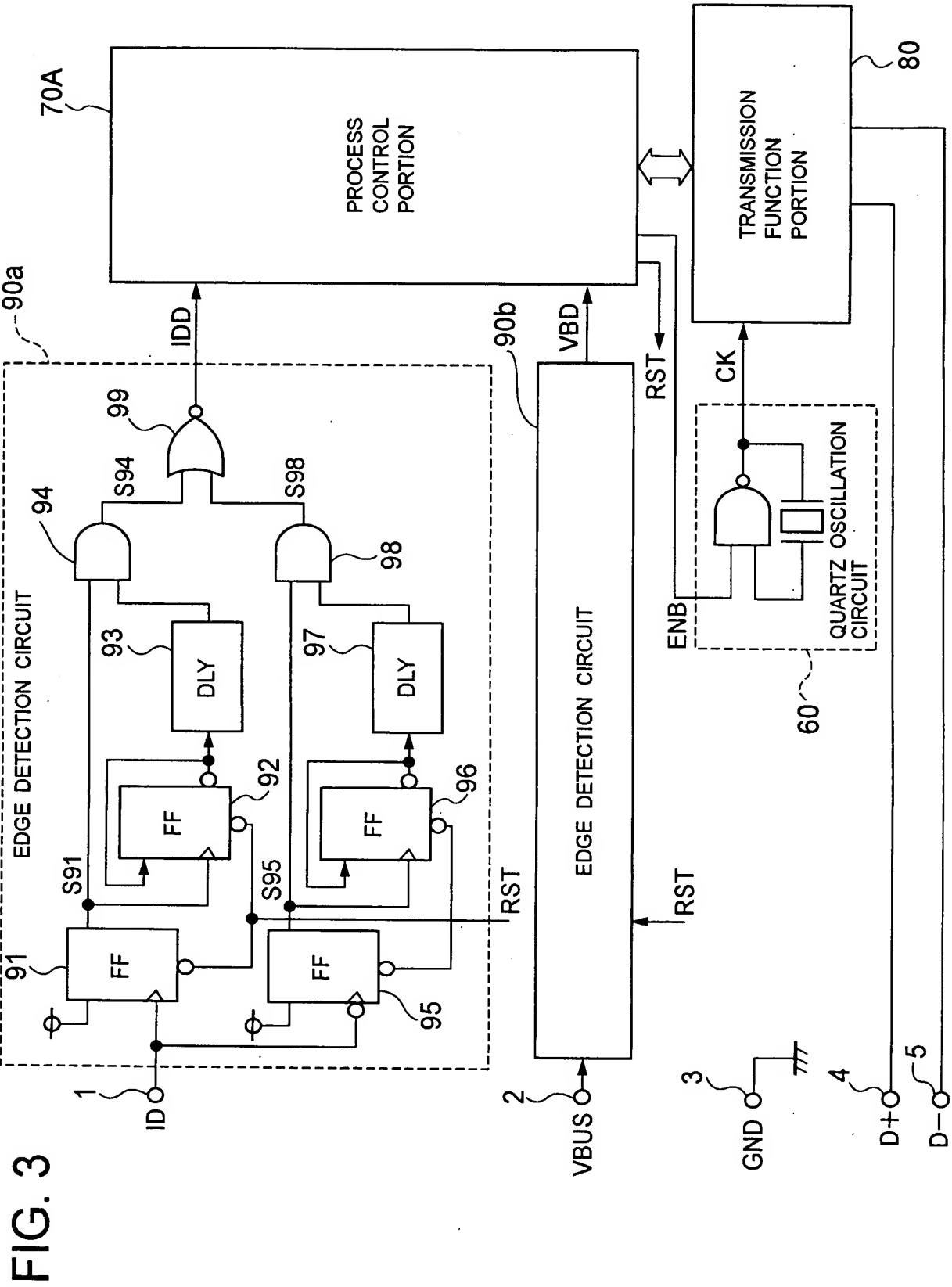


FIG. 4

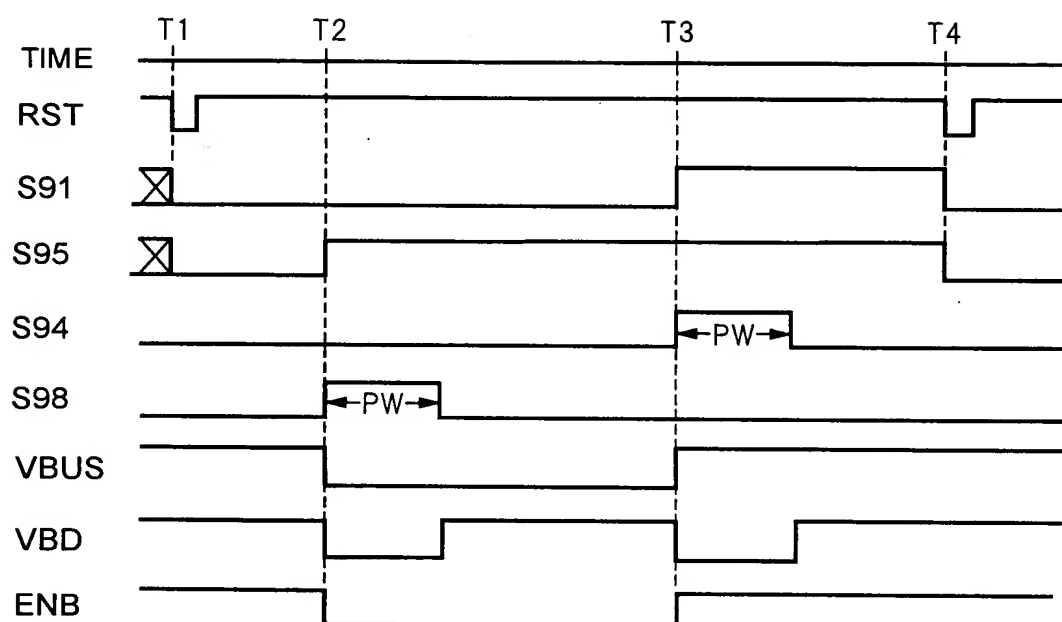


FIG. 5

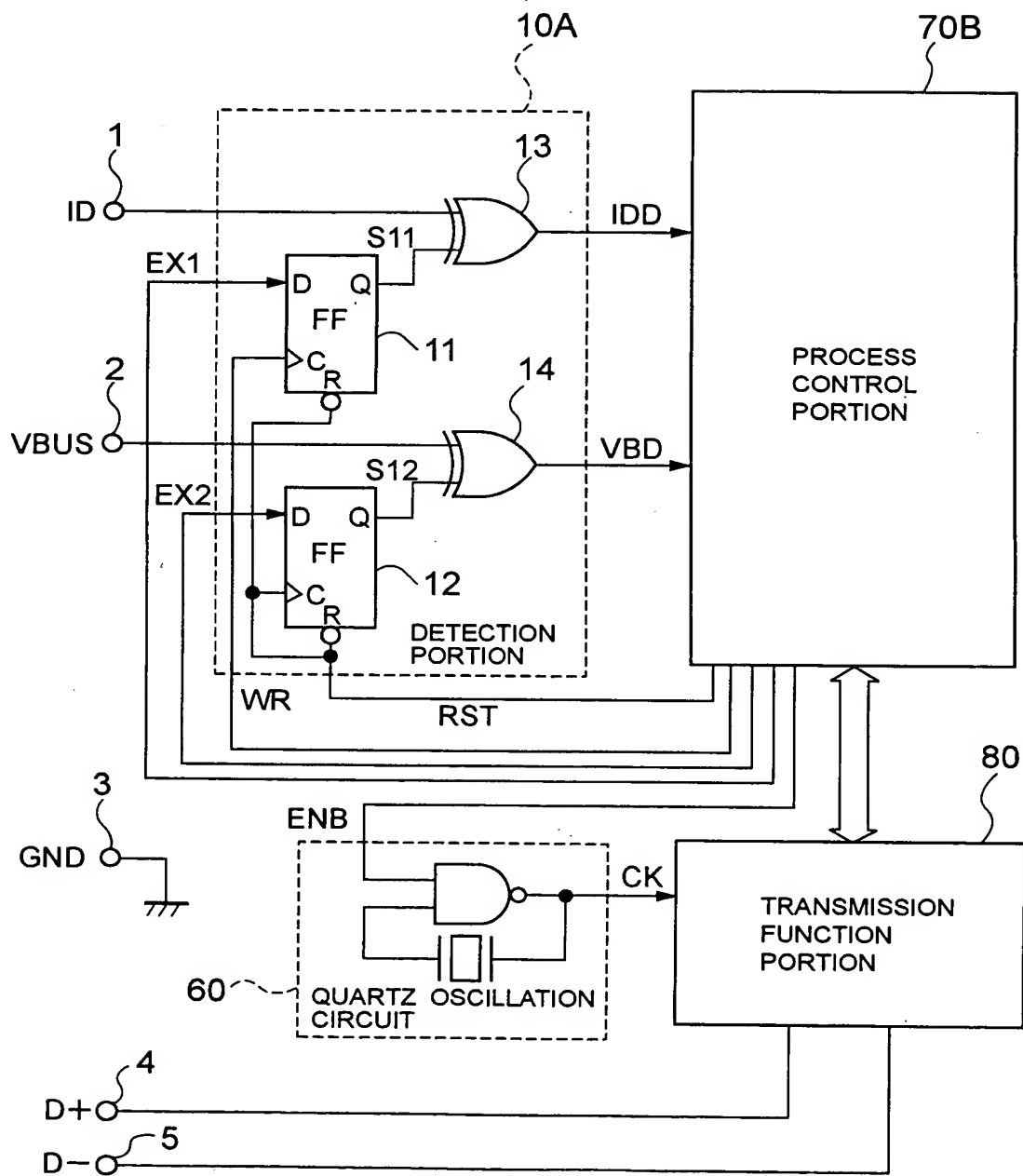




FIG. 7

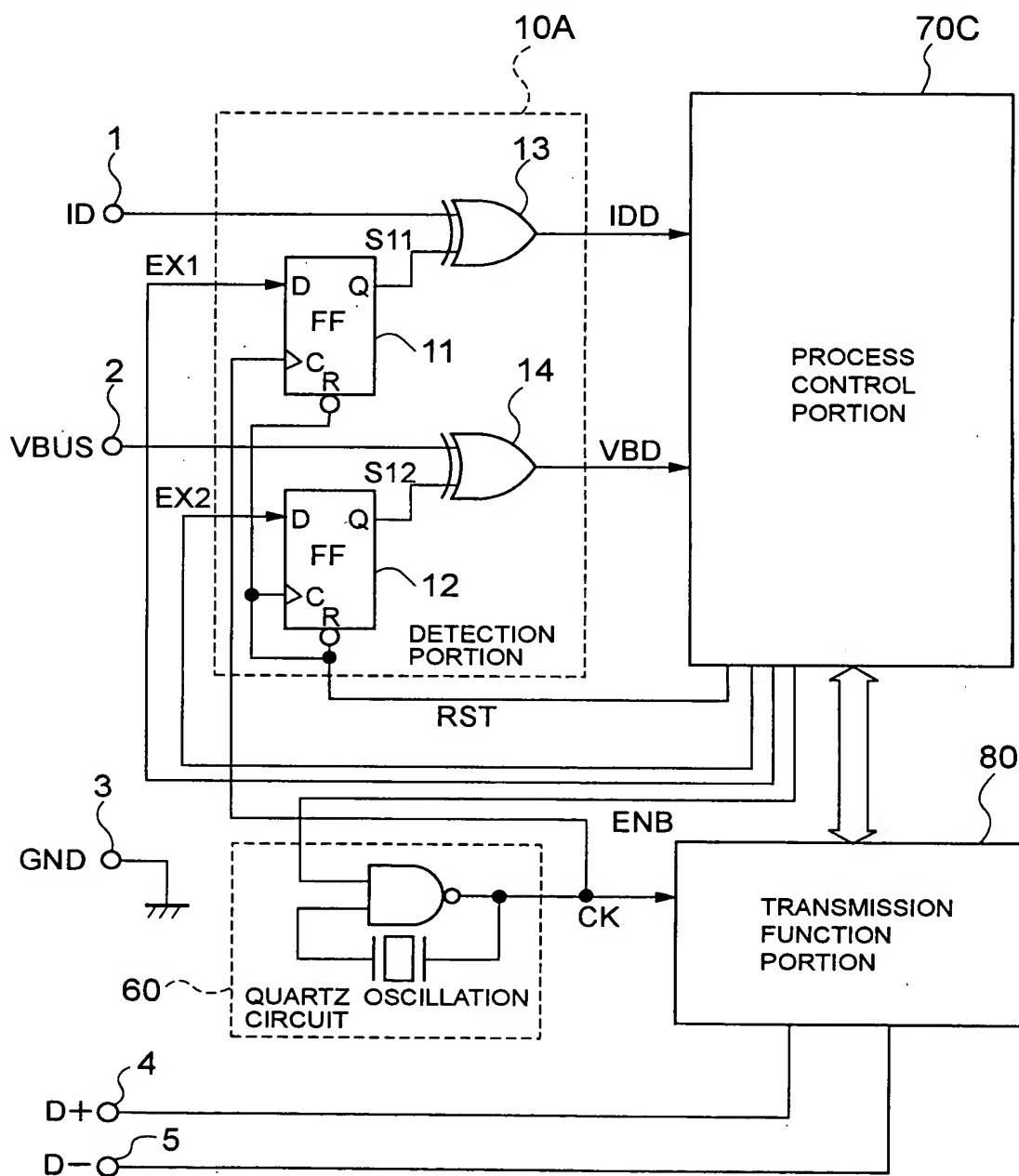


FIG. 8

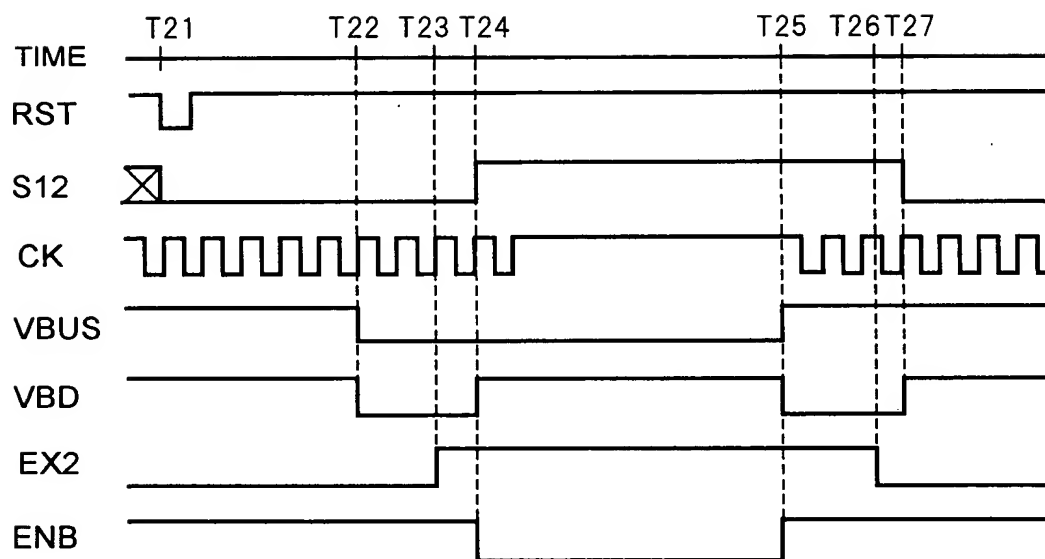




FIG. 9

